The Electronics System in the Daya Bay Experiment

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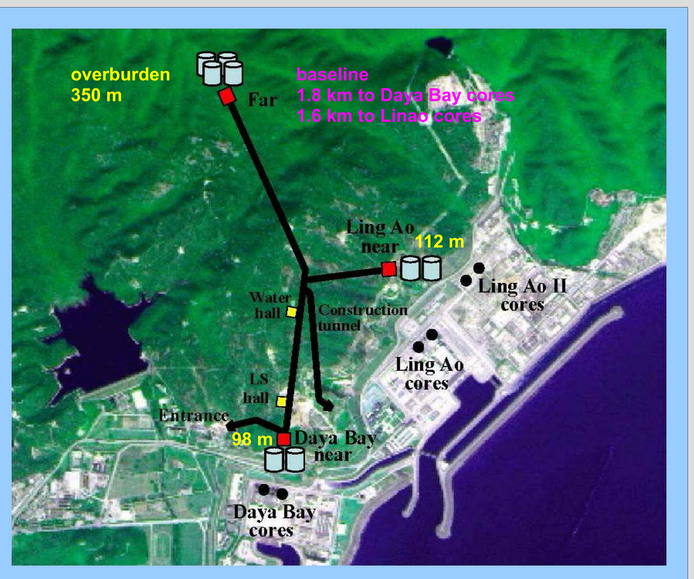
Introduction to the Daya Bay experiment

The Daya Bay collaboration has more than 200 collaborators from Asia, North America, and Europe.

The experiment is located in south-east china, 55 km away from central Hong Kong.

The experimental goal is to observe the neutrino mixing angle θ_{13} with a precision of $\sin^2(2\,\theta_{13})=0.01$ in a three-year run. A dry-run of the first anti-neutrino detector without liquid scintillator is expected to start in fall 2009.



The Daya Bay nuclear power complex. The Daya Bay NPP is in the foreground. The Lingao NPP is in the background. The experimental halls are inside the hills to the left.

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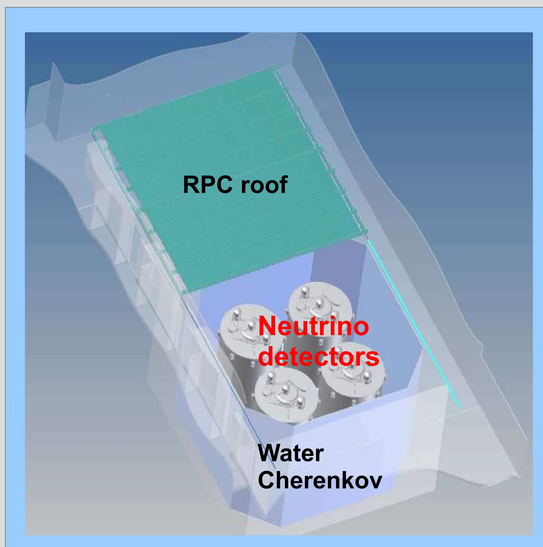
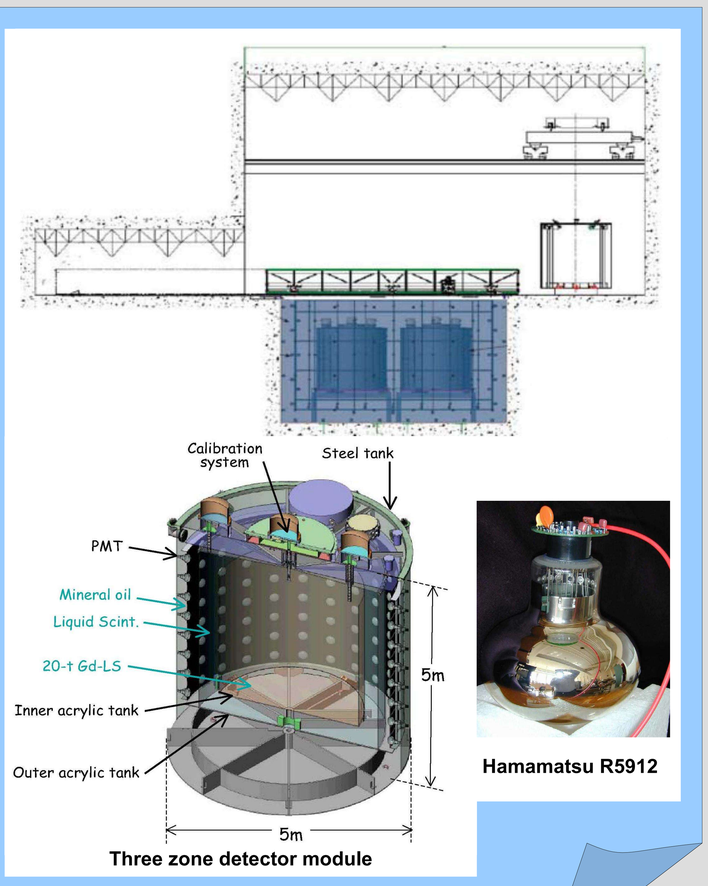
Neutrino and Muon Detectors layout



Anti-neutrino Detector (AD):
20 ton 0.1% Gd-doped Liquid Scintillator (Gd-LS) target with 192 PMTs per module. 4 modules for far site and 2 for near sites.

Muon Detector (MD):
2-layer Water Cherenkov.
4-layer Resistive Plate Chamber (RPC) roof.



Three zone detector module

Hamamatsu R5912

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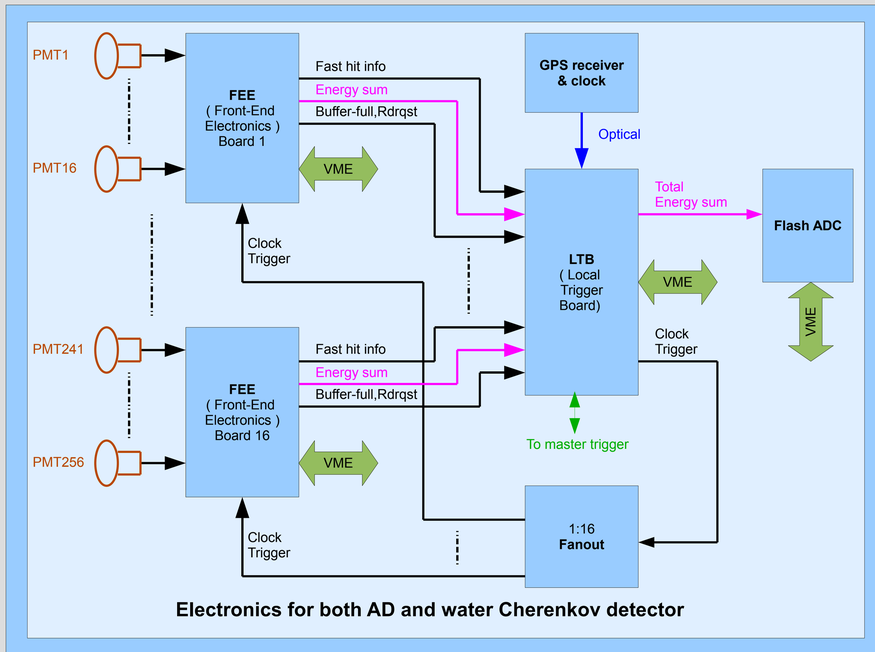
The Daya Bay electronics subsystem



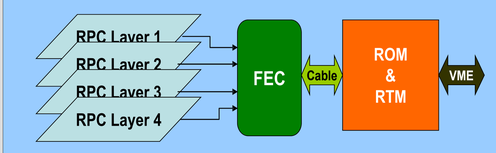
Electronics for both AD and water Cherenkov detector

Since both AD and water Cherenkov detector are PMT based, an identical readout electronics subsystem is developed.

Up to 16 Front End Electronics (FEE) modules, one Local Trigger Board (LTB), one flash ADC, and one Fanout module can be equipped in a VME crate. The subsystem can handle up to 256 PMTs.

All modules work with a synchronize clock. Each event has a time stamp.

Multiplicity trigger and energy-sum trigger are implemented in the LTB.



RPC electronics

A master trigger module is also being developed to have cross check between AD and MD.

RPC electronics consists of Front End Card (FEC), Read Out Module (ROM) and RPC Trigger Module (RTM).
RPC works independently on a self trigger mode. The muon signature is 3 out of 4.

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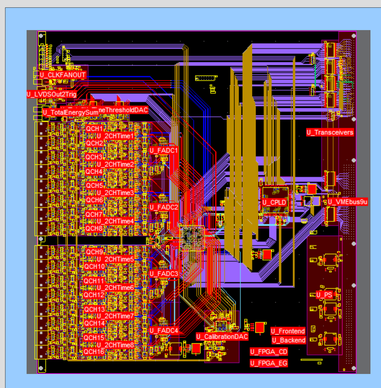
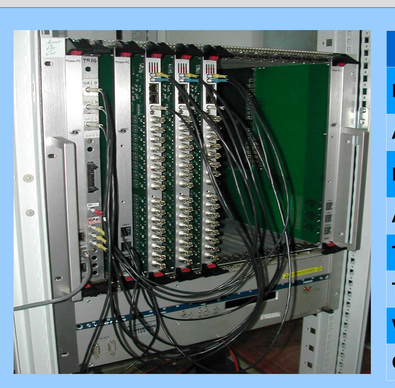
FEE overview



FEE PCB: 8 layer VME module



3 prototype FEE modules under testing

Quantity	Specification
Dynamic Rang	0~400 p.e. for fine range 0~4000 p.e. for coarse range
ADC bit resolution	10% @ 1 p.e.
No. of ADC bits	12 for fine range 12 for coarse rang
ADC Sampling rate	40 MSPS
Time range	0~500 ns
Time Precision (rms)	500 ps
VME standard	VME64xp 9U-340 mm
Channel per board	

Daya Bay FEE is a VME 9U module, which can handle up to 16 channels of PMT outputs. 16 channels of dual range 12 bit ADC and 16 channels of 20 bit TDC are integrated.

The waveform of each input pulse will be sampled with a 40 MHz clock after a shaping circuit. The TDC utilizes a 320 MHz clock. A trigger issued by the LTB is the common stop signal for all the TDC channels.

The event information along with ADC and TDC data will be stored in the buffer inside the onboard FPGA.

The VME controller reads data from each FEE via VME bus using a Chained Block Transfer (CBLT) mode after a data-ready interrupt signal asserts.

Some specifications of the FEE are listed on the table above.

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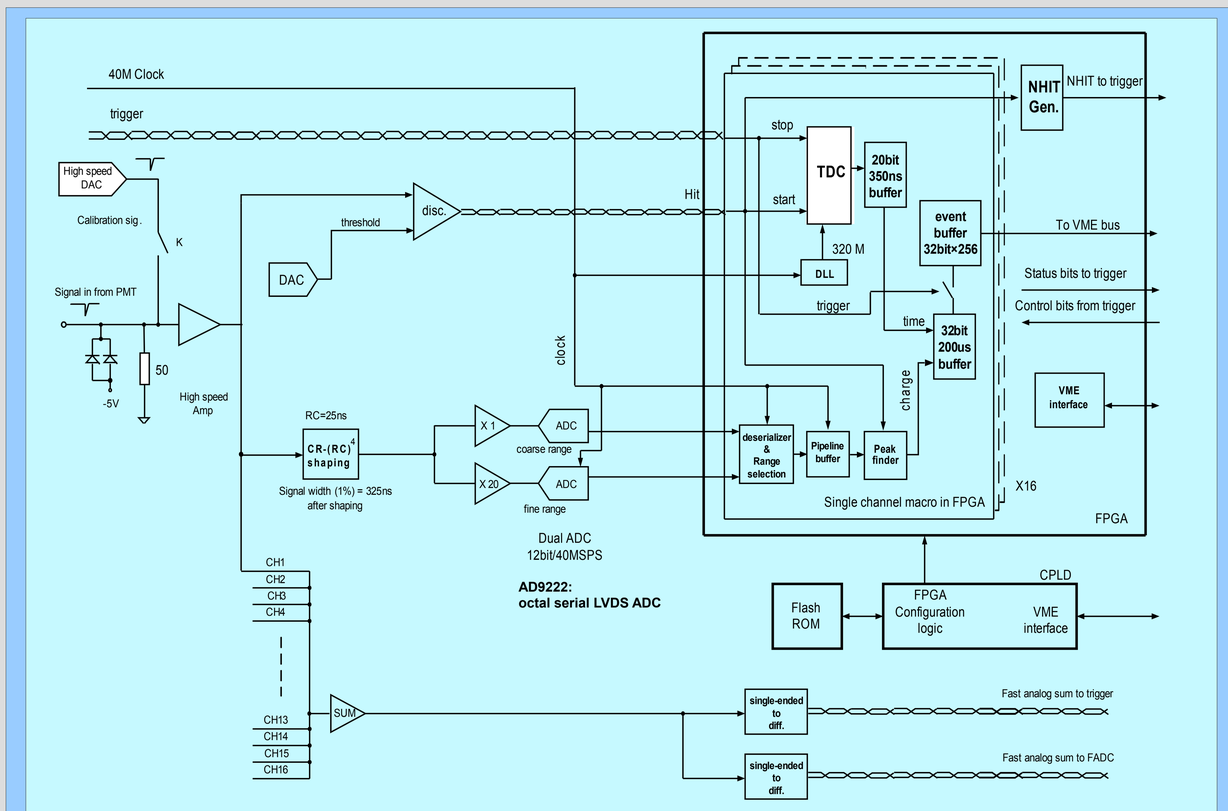
FEE block diagram



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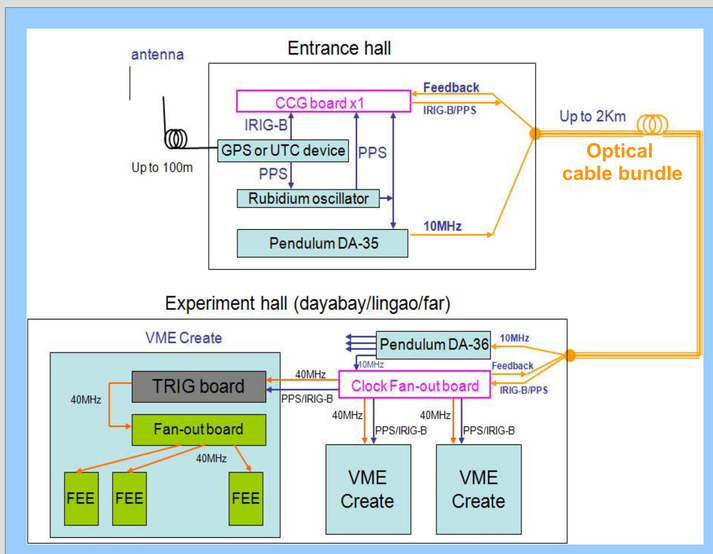
The Daya Bay Clock system



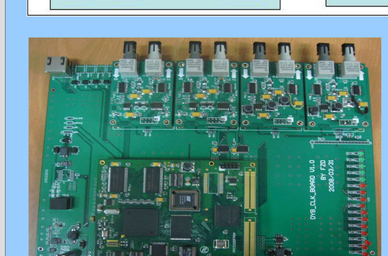
A 10 MHz clock and the absolute time base on a Central Clock Generator (CCG) are generated in the control room outside of the tunnel

The 10 MHz clock is broadcast to each underground experimental hall by a Pendulum transceiver.

The absolute time with a precise Pulse Per Second (PPS) signal will be modulated and sent with compensation, so that the cable length difference can be ignored.

The 10 MHz clock is multiplied into 40 Mhz in the Clock Fan-out Board before applying to each LTB.

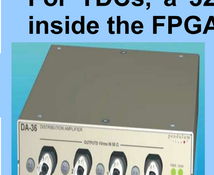
In the FEE, ADCs run under 40 MHz clock. For TDCs, a 320 MHz clock is generated inside the FPGA on the FEE.



Central Clock Generator

Symatricom Rubidium Clock (10 ps Jitter)

Symatricom GPS (200 ns precise PPS)



Pendulum clock transceiver (50 ps)

Clock Fan-out Board

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