The Trigger System in Daya Bay neutrino experiment

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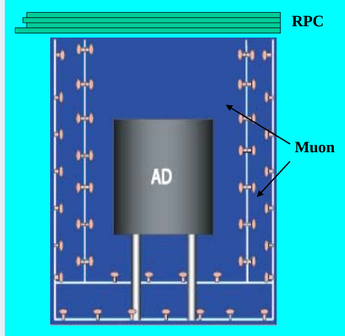
Overview of the Trigger System

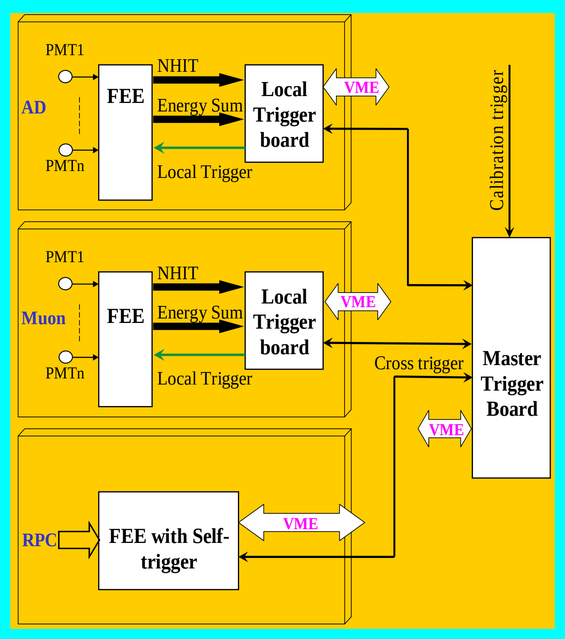


The Daya Bay neutrino experiment employs 3 types of sub-detectors: the anti-neutrino detector (AD), the water Cerenkov detector (MUON) and the resistive plate chambers (RPC).

Since both the AD and the Muon output the photomultiplier-tube (PMT) signals, Identical front-end electronics board (FEE) and local trigger board (LTB) are used.

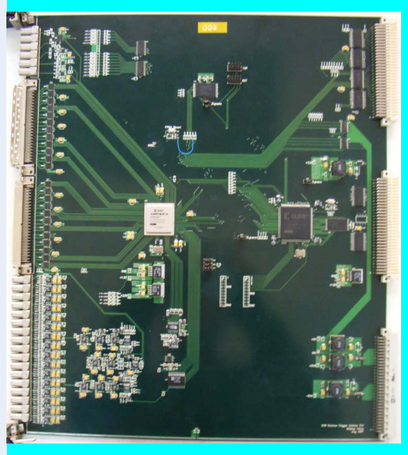
One FEE can receive 16 PMT signals at most and generate the number of coincident PMT hits (NHIT) and the total analog sum of 16 PMTs input signals (ESUM) .

One LTB can process the NHIT and ESUM signals from 16 FEEs and generate local trigger and cross trigger.

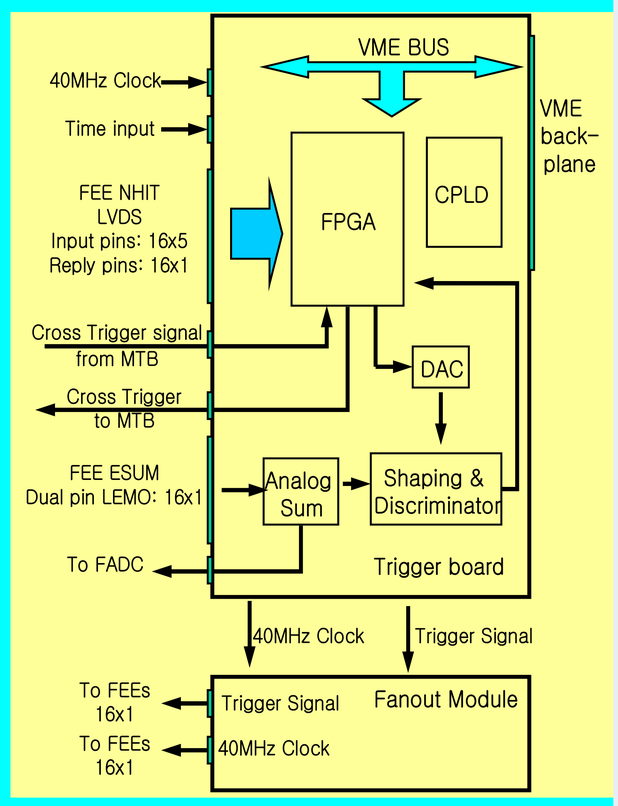


To let the cross trigger generated from one sub-detector be sent to the other sub-detectors, a master trigger board (MTB) is designed.

Architecture of Local Trigger Board



LTB is designed as a 9U VME standard slave module.



LTB handles the following data sources: HSUM and ESUM signals from FEEs; the calibration trigger and the cross trigger from the MTB; the internal periodic trigger.

LTB receives time information and 40MHz clock signal from the clock system.

Both the clock signal and the local trigger signal are sent to the 16 FEE boards via a fan-out module.

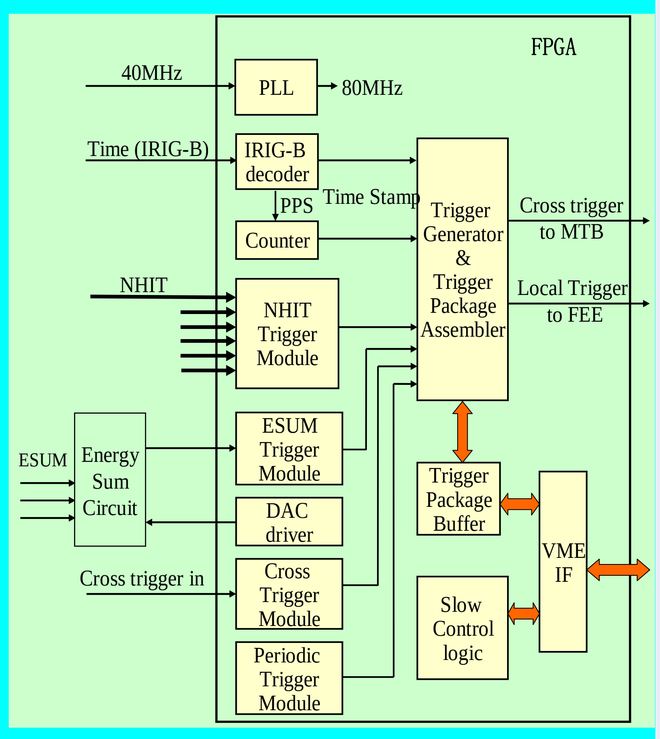
Local trigger board Firmware

An absolute time information is distributed to LTB via a single serialized input signal every second, which is encoded in the IRIG-B format.

Inside the FPGA, 4 modules make inner trigger decisions: the NHIT trigger module, the ESUM trigger module, the cross trigger module and the periodic trigger module.

These 4 inner triggers are ORed to generate local trigger and cross trigger.

For each local trigger, the time stamp, source data and trigger type are packed into a trigger data package.



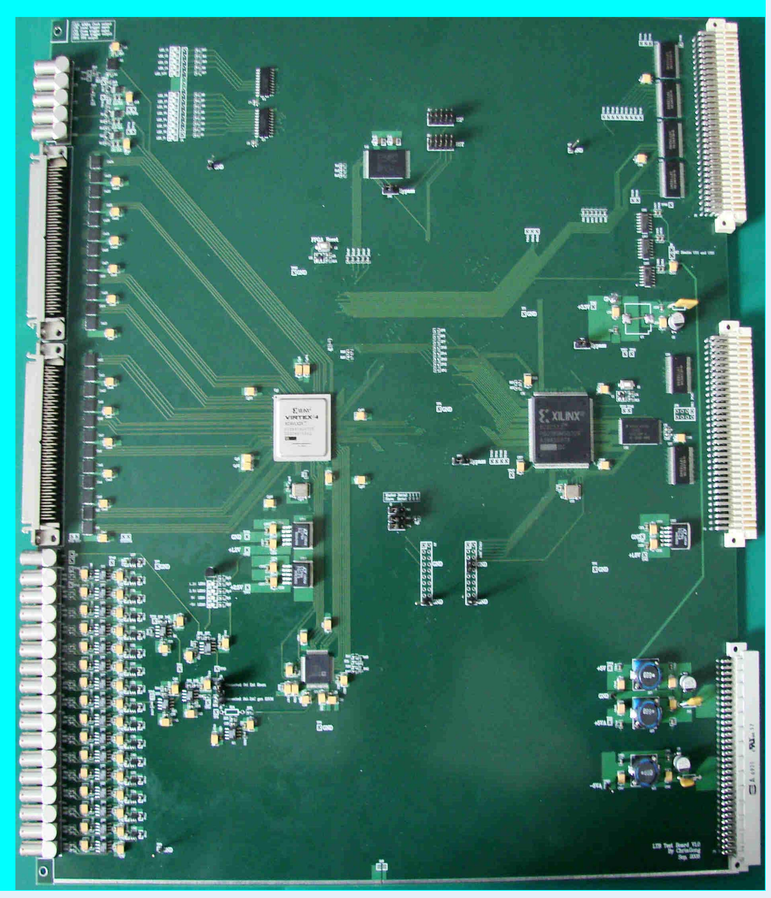
The 4 inner trigger signals are generated with a different but fixed processing latency. In order to obtain identical trigger latency for each inner trigger, a trigger latency correction is introduced and controlled via VME interface.

Trigger TEST board

In order to test LTB hardware and firmware, a trigger test board (TTB) is specially developed.

This test board has the same dimension, adopts the identical FPGA chip and works as a VME slave module as well.

The number and the type of interfaces are the same as the trigger board except for the inverted direction.



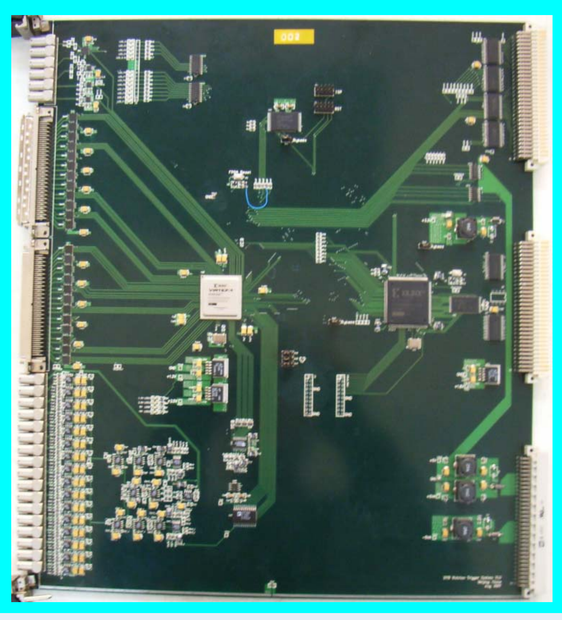
Master trigger board

Master trigger board = LTB + interface board

Interface board converts one 100-pin D-type interfaces to many dual-pin LEMO interface, which is used to receive or transmit cross trigger signals.

Interface board is a rather simple board and is not programmable.

The firmware of Master trigger board is under design.

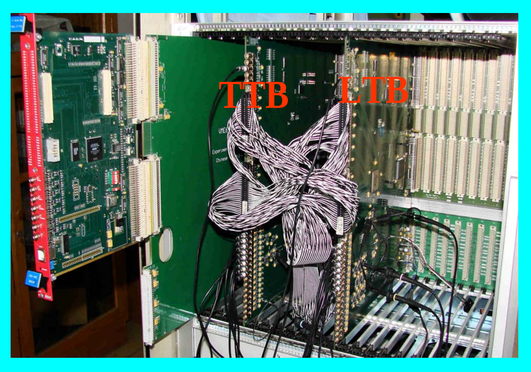


LTB

+

Interface Board

Test of Trigger system

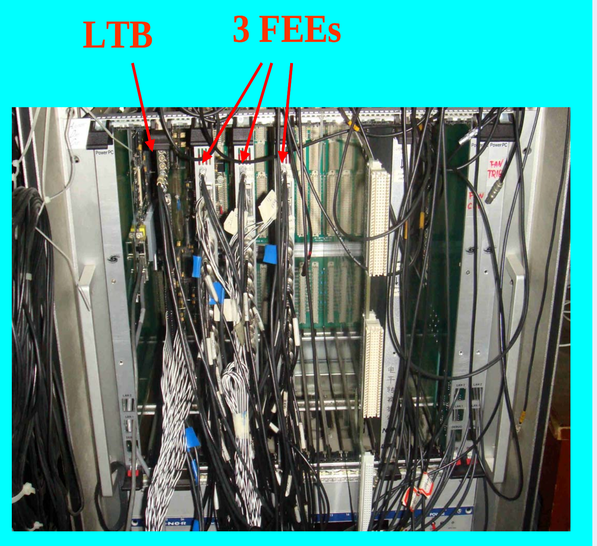


A simple experiment has been made to test the trigger efficiency of LTB.

In this experiment, TTB outputs NHIT signals and counts the number of valid NHIT signals.

LTB receives NHIT signals, generates local triggers and counts the number of local triggers.

Via VME interface, two counting numbers are readout and founded to be identical.



In addition, LTB is under testing now in a prototype experiment, which consists of one LTB, 3 FEE boards and the DAQ system.

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